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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/848,816	05/18/2004	Hideki Yuzawa	9319S-000791	4802

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/848,816	YUZAWA, HIDEKI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

2. Figures 4A and 4B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

3. The disclosure is objected to because of the following informalities: page 1, paragraph [0005], line 3, the word "fro" appears to be a typographical error. The sentence on paragraph [0034], lines 9-11 is confusing. Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

5. Claims 1 and 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scopes of claims 1 and 5-7 are unclear as to what the limitation of "first projected electrodes each having a first center disposed on a first line linking the first centers; and a second projected electrodes each having a second center disposed on a second line linking the second centers" actually mean in relation to the claimed first and second projected electrodes. And it is not clear where the lines are formed and they are spaced apart in relation to each other.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikebe, US patent No. 5,569,964.

Regarding claim 1, Ikebe teaches (figs. 12-13 and 20) a semiconductor device, comprising: a semiconductor chip (16) a first projected electrode array (17A) projecting from and disposed on a surface of the semiconductor chip (refer to fig. 13), the first projected electrode array including a plurality of first projected electrodes each having a first center (a line that cuts top 17A in half and goes all the down) disposed on a first line linking the first centers and a second projected electrode array (17B) projecting from and disposed on the surface of the semiconductor chip (refer to fig. 13), the second projected electrode array including a plurality of a second projected electrodes (17A) each having a second center disposed on a second line (a line that cuts top 17B in half

and goes all the down) linking the second centers, wherein: the first line and the second line are laterally spaced apart a width (Bw1) of each first projected electrode is smaller than a width (Bw2)of each second projected electrode and a length (Bd1) of each first projected electrode (17A) is longer than a length (d2) of each second projected electrode.

Regarding claim 2, Ikebe teaches the entire claimed structure of claim 1 above including each first projected electrode (17A) and each second projected electrode (17B) are substantially equal to each in a surface area facing a wiring board (refer to table 2).

Regarding claim 3, Ikebe teaches the entire claimed structure of claim 1 above including a wiring board on which the semiconductor chip (16) is mounted and a wiring pattern (15) connected to the first and the second projected electrodes and disposed on the wiring board (region where the chip 16 sits, refer to figs. 12 and 13).

Regarding claim 4, Ikebe teaches the entire claimed structure of claim 1 above including wherein a resin layer (18) is provided between, the semiconductor chip (16) and the wiring board (region where the chip 16 sits, refer to figs. 12 and 13).

Regarding claims 5 and 6, Ikebe teaches (figs. 12-13 and 20) an electronic device (electronic equipment) comprising an electronic component (semiconductor chip 16); a first projected electrode array (17A) projecting from and disposed on a surface of the electronic component (16), the first projected electrode array including a plurality of first projected electrodes (17A) each having a first center (a line that cuts top 17A in half and goes all the down) disposed on a first line linking the first centers; and a second

projected electrode (17B) array projected from and disposed on the surface of the electronic component (16), the second projected electrode array including a plurality of second projected electrodes each having a second center disposed on a second line linking the second centers (a line that cuts top 17B in half and goes all the down), wherein the first line and the second line are laterally spaced apart a width (Bw1) of each first projected electrode is smaller than a width (bw2) of each second projected electrode and a length (Bd1) of each first projected electrode is longer than a length (Bd2) of each second projected electrode.

Regarding claim 7, Ikebe teaches (figs. 12-13 and 20) a method of manufacturing a semiconductor device that includes first (17A) and second projected electrode (17B) arrays projecting from and disposed on a semiconductor chip (16), the method comprising: providing the first projected electrode array by disposing a plurality of first projected electrodes (17A) on the semiconductor chip (16), each first projected electrode having a first center disposed on a first line linking the first centers (a line that cuts top 17A in half and goes all the down), providing the second projected electrode array (17B) by disposing a plurality of second projected electrodes on the semiconductor chip (16), each second projected electrode having a second center disposed on a second line linking the second centers (a line that cuts top 17B in half and goes all the down); mounting the semiconductor chip (16) on a wiring board (region where the chip 16 sits, refer to figs. 12 and 13) where a wiring pattern (15) is disposed through the first and second projected electrode arrays and electrically connecting the wiring pattern to the first and the second projected electrode arrays (17A and 17B)

wherein a width (Bw1) of each first projected electrode is smaller than a width (Bw2) of each second projected electrode and a length (Bd1) of each first projected electrode is longer than a length (Bd2) of each second projected electrode.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A and B are cited as being related to a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
February 5, 2005

EDDIE LEE
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